Doc. Version	0.5
Total Page	25
Date	2006/11/30

Product Specification

6.5" COLOR TFT-LCD MODULE

MODEL NAME: C065VL01 V0

<◆>Draft Version
< >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change

Record of Revision

Version	Revise Date	Page	Content
0.0	2006/02/10		First draft.
0.1	2006/06/01	5	D-1-a updated connector type, pin number & pin assignment
		9	D-3-c updated LED voltage, current and life time
		13	E updated response time
		16	G updated drawing
		18	Added typical application circuit and power on/off sequence
0.2	2006/07/21	5	Revise connector type, pin number & pin assignment
		14	Revise Viewing angle typical value in Optical characteristics
		17	Update outline drawing
		19	Revise application note
		21	Revise power on/off sequence
0.3	2006/09/06	10	Revise LED backlight driving voltage
0.4	2006/10/03	10	Revise AVDD & VGH typical value
		19-24	Update Application Notes contents
0.5	2006/11/30	10	Revise AVDD values
		25	Add important note for customer system design

Contents

A. Summary 4
B. Features 4
C. Physical Specifications 4
D. Electrical Specifications 5
1. Pin Assignment 5
2. Absolute Maximum Ratings 9
3. Electrical Characteristics 10
E. Optical specifications 14
F. Reliability Test Items 16
G. Outline Dimension 17
H. Packing Form 18
I. Application Notes 19
1. Typical Application Circuit 19
2. Power On/Off Sequence 21

A. Summary

C065VL01 is an LTPS (Low Temperature Poly-Silicon) type TFT (Thin Film Transistor) LCD (Liquid crystal Display). This model is composed of a TFT-LCD panel, a driver IC, a FPC (flexible printed circuit), and a backlight unit.

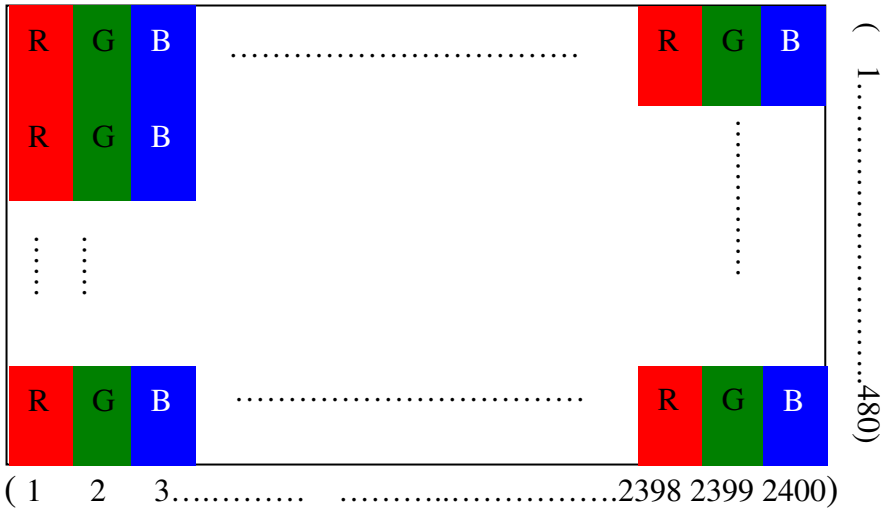
B. Features

- 6.5” display size in 16:9 aspect ratio
- 800RGBx480(WVGA) resolution for wide view format
- 550nits high brightness with high power LED backlight
- 300:1 high contrast
- Wide viewing angle technology, best at 6 o’clock direction
- Parallel RGB I/F of 6-bit color depth
- Power supply: 3.3V for panel and 13.2V for LED

C. Physical Specifications

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	800RGB(H)×480(V)	
2	Active Area	mm	143.40(H)×79.2(V)	
3	Screen Size	inch	6.5(Diagonal)	
4	Pixel Pitch	mm	0.05975×RGB(H)×0.165(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	262K Colors	Note 2
7	Overall Dimension	mm	157.2(H) × 89.2(V) × 5.3(T)	Note 3
8	Weight	g	120±5%	
9	Panel surface treatment	--	AG(25% haze) & with SWV film	
10	Display Mode	--	Normally White	
11	Backlight Unit	--	High Power LED’s	

Note 1: Below figure shows the dot stripe arrangement.



Note 2: The 262K color display depends on 6-bit data signal input.

Note 3: Not including the backlight cable. Refer to Section G, “Outline Dimension” for further information.

D. Electrical Specifications

1. Pin Assignment

a. TFT-LCD panel driving section

Connector type: FH16-80S-0.3SH or compatible

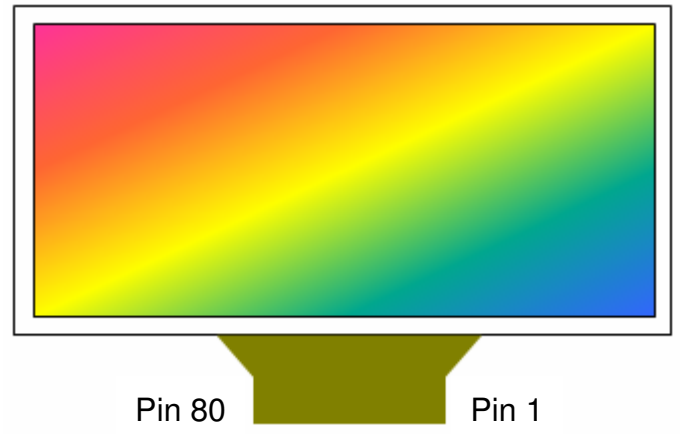
Pin no	Symbol	I/O	Description	Remark
1	VGH	P	Power for LCD	
2	DIO2	I/O	Start pulse signal	
3	AVDD	P	Analog power for source driver	
4	CHNSL1	I	Control signal, please set to ‘1’	
5	CHNSL0	I	Control signal, please set to ‘1’	
6	VCC	P	Digital power for source driver	
7	POL	I	Output data polarity control signal	
8	REV	I	Data inversion control signal output for source driver	
9	LINV	I	Polarity control signal	
10	MUX2	I	Source driver control signal	

11	MUX1	I	Source driver control signal	
12	MUX0	I	Source driver control signal	
13	GAMA	I	Source driver control signal ,please set to ‘1’	
14	LD2	I	Source driver control signal	
15	LD1	I	Source driver control signal	
16	OP1	I	Output buffer driving capacity control signal	
17	OP0	I	Output buffer driving capacity control signal	
18	MODE	I	Control signal , please set to ‘1’	
19	GND	P	Digital ground	
20	B5	I	Blue data	
21	B4	I	Blue data	
22	B3	I	Blue data	
23	B2	I	Blue data	
24	B1	I	Blue data	
25	B0	I	Blue data	
26	GND	P	Digital ground	
27	AGND	P	Analog ground	
28	V14	P	Gamma reference voltage	
29	V13	P	Gamma reference voltage	
30	V12	P	Gamma reference voltage	
31	V11	P	Gamma reference voltage	
32	V10	P	Gamma reference voltage	
33	V9	P	Gamma reference voltage	
34	V8	P	Gamma reference voltage	
35	V7	P	Gamma reference voltage	
36	V6	P	Gamma reference voltage	
37	V5	P	Gamma reference voltage	
38	V4	P	Gamma reference voltage	
39	V3	P	Gamma reference voltage	
40	V2	P	Gamma reference voltage	
41	V1	P	Gamma reference voltage	
42	AVDD	P	Analog power for source driver	
43	GND	P	Digital ground	
44	G5	I	Green data	
45	G4	I	Green data	
46	G3	I	Green data	

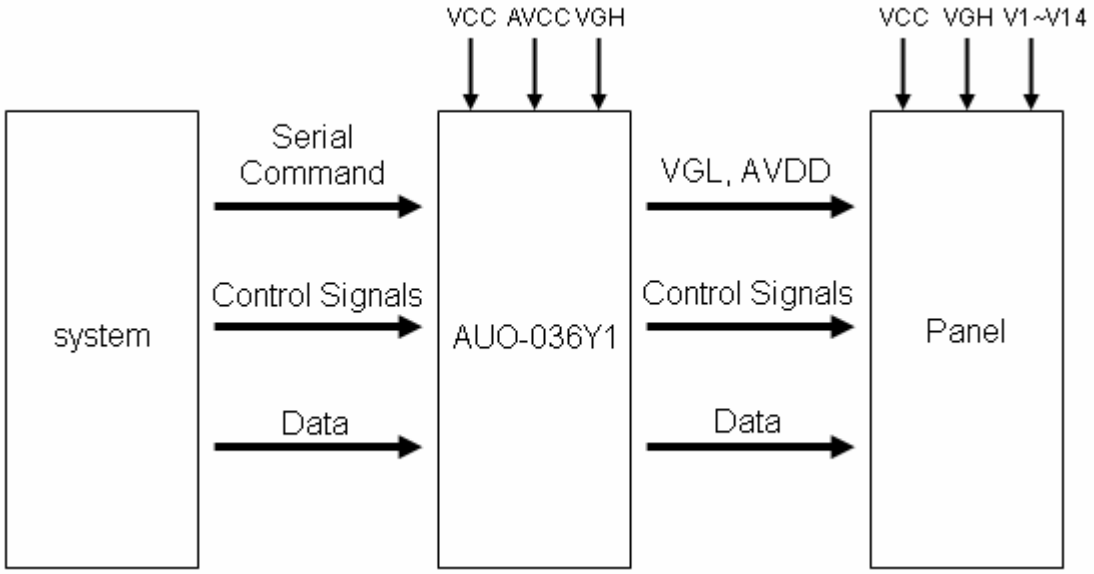
47	G2	I	Green data	
48	G1	I	Green data	
49	G0	I	Green data	
50	GND	P	Digital ground	
51	R5	I	Red data	
52	R4	I	Red data	
53	R3	I	Red data	
54	R2	I	Red data	
55	R1	I	Red data	
56	R0	I	Red data	
57	GND	P	Digital ground	
58	PRSEL1	I	Source driver control signal , please set to ‘0’	
59	PRSEL0	I	Source driver control signal , please set to ‘1’	
60	SHL	I	Source driver horizontal shift direction control	
61	CLK	I	Output data clock for source driver	
62	EDGSL	I	Source driver control signal	
63	RSTB	I	Reset pin, low active	
64	VCC	P	Digital power for source driver	
65	AGND	P	Analog ground	
66	DIO1	I/O	Start pulse signal	
67	SW6	I	Control signal	
68	SW5	I	Control signal	
69	SW4	I	Control signal	
70	SW3	I	Control signal	
71	SW2	I	Control signal	
72	SW1	I	Control signal	
73	VGL	P	Power for LCD	
74	VGH	P	Power for LCD	
75	CK	I	Control signal	
76	XCK	I	Control signal	
77	VST	I	Control signal	
78	NC		not connected	
79	NC		not connected	
80	VCOM	I	Common electrode voltage	

I: Input pin; O: Output pin; P: Power pin

Note1: For pin sequence arrangement, please refer to the figure as below:



b. Block Diagram



c. Backlight driving section

Connector type: JST PHR-2 or compatible

No.	Symbol	I/O	Description	Remark
1	GND	-	Ground for backlight unit	--
2	HI	I	Power supply for backlight unit (High voltage)	--

2. Absolute Maximum Ratings

Items	Symbol	Product Specification			Unit
		Min.	Typ.	Max.	
Power Voltage	VCC	-0.3		4	V
	AVDD	-0.5		13.5	V
	VGH	-0.5		17	V
	VGL	-17		0.5	V
	VGH-VGL	-0.5		26.5	V
Input Signal Voltage	Vin	-0.3		VCC+0.3	V
	VCOM	-	-	-	V
Operating Temperature	Topa	-30		85	˚C
Storage Temperature	Tstg	-40		95	˚C

3. Electrical Characteristics

a. Typical operating conditions

Items	Symbol	Product Specification			Unit
		Min.	Typ.	Max.	
Power Voltage	VCC	3.0	3.3	3.6	V
	AVDD	8	10.5	12	V
	VGH	10	13.5	15	V
	VGL	-5	-7	-9	V
	VCOM	0.35*AVDD	0.5*AVDD	0.65*AVDD	V
Input H/L level Voltage	VIH	0.7*VCC	—	VCC	V
	VIL	0	—	0.3VCC	V

Note 1: All value should be measured under the condition of GND=AVss=0V

Note 2: The panel is designed to prevent the current leakage for the best display performance. If shorter discharge time is desired when system power off, then extra discharge circuit may be required at customer's side.

b. Current Consumption

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current For Driver	IGH	VGH=12V		TBD		uA
	IGL	VGL=-7V		TBD		uA
	ICC	VCC=3.3V		TBD		mA
	IDD	AVDD=10V		TBD		mA

c. LED Backlight driving condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage	Vf	Note 1		16.5	TBD	Vrms
Current	If	Note 1			150	mA
LED life time		Note 2	10000	-		Hrs

Note 1: Panel surface temperature should be kept less than content of "D.2. Absolute maximum ratings".

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃, If=150mA

d. AC Timing Conditions

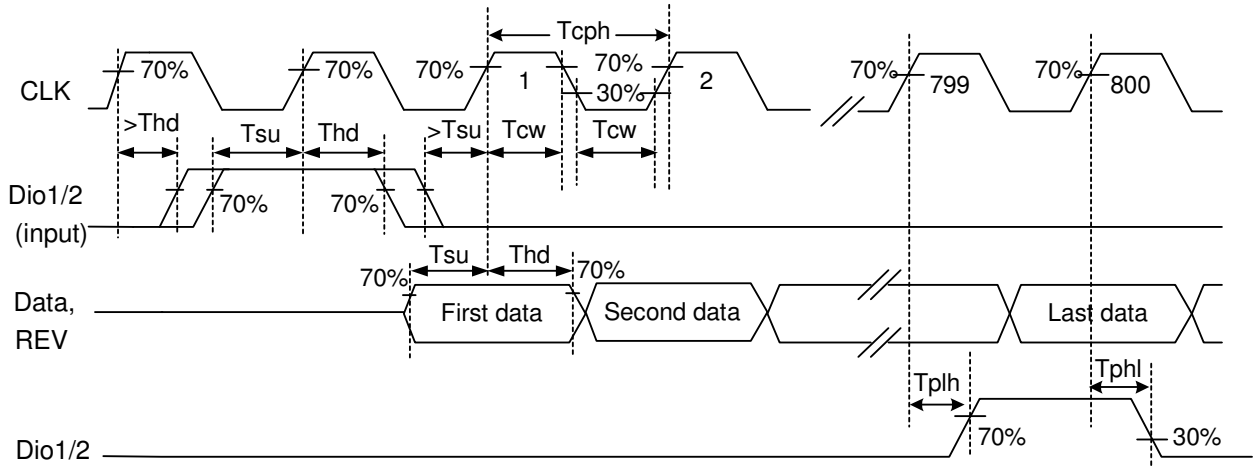
Characteristics (VCC=3V, AVDD=10V, AVSS=GND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
CLK frequency	Fclk=1/Tclk	-	-	45	MHz	EDGSL="0"	
CLK frequency	Fclk=1/Tclk	-	-	22.5	MHz	EDGSL="1"	
CLK pulse width	Tcw	6	-	-	ns		
Data set-up time	Tsu	4	-	-	ns	X1 ~ X5, REV and DIO1/2 to CLK	
Data hold time	Thd	2	-	-	ns		
Propagation delay of DIO1/2 high to low level	Tphl	6	10	15	ns	CL=25pF	
Propagation delay of DIO1/2 low to high level	Tplh	6	10	15	ns	CL=25pF	
Time that the last data to LD1	Tld1	1	-	-	Tclk		
LD1 pulse width	Twld1	2	-	-	Tclk		
Time that LD1 to DIO1/2	Tlds	5	-	-	Tclk		
Time that LD1 to LD2	Tld2	2	-	-	Tclk		
LD2 pulse width	Twld2	1	-	-	Tclk		
MUX/LINV/POL setup time	Tsu2	6	-	-	ns		
MUX/LINV/POL hold time	Thd2	6	-	-	ns		
Output stable time	Tst	-	-	-	us	Refer to LD2 timing chart	

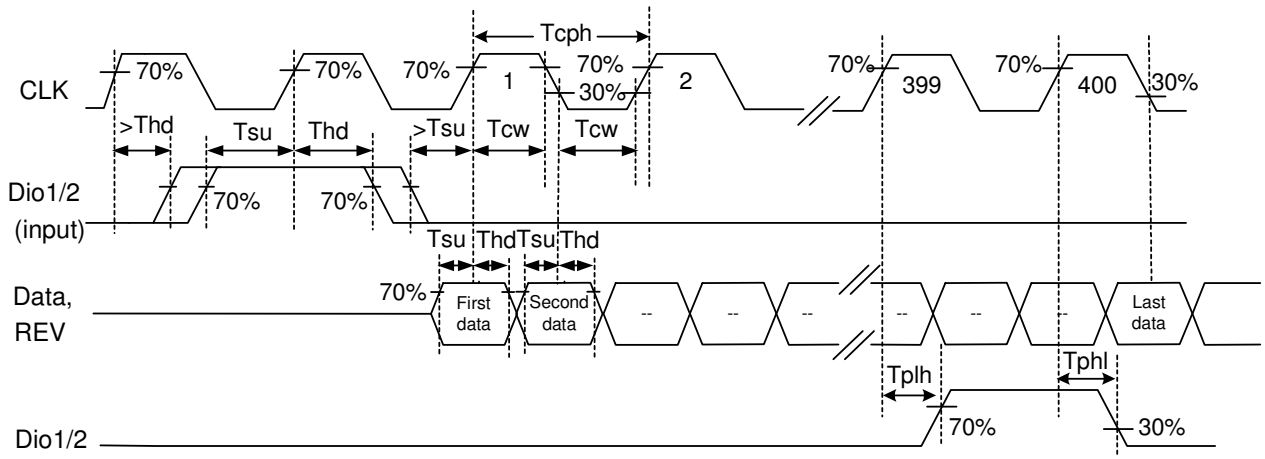
e. Timing Diagrams

Timing Diagram 1 (CHNSL="1", others setting = Default)

<< EDGSL= "0", Default >>

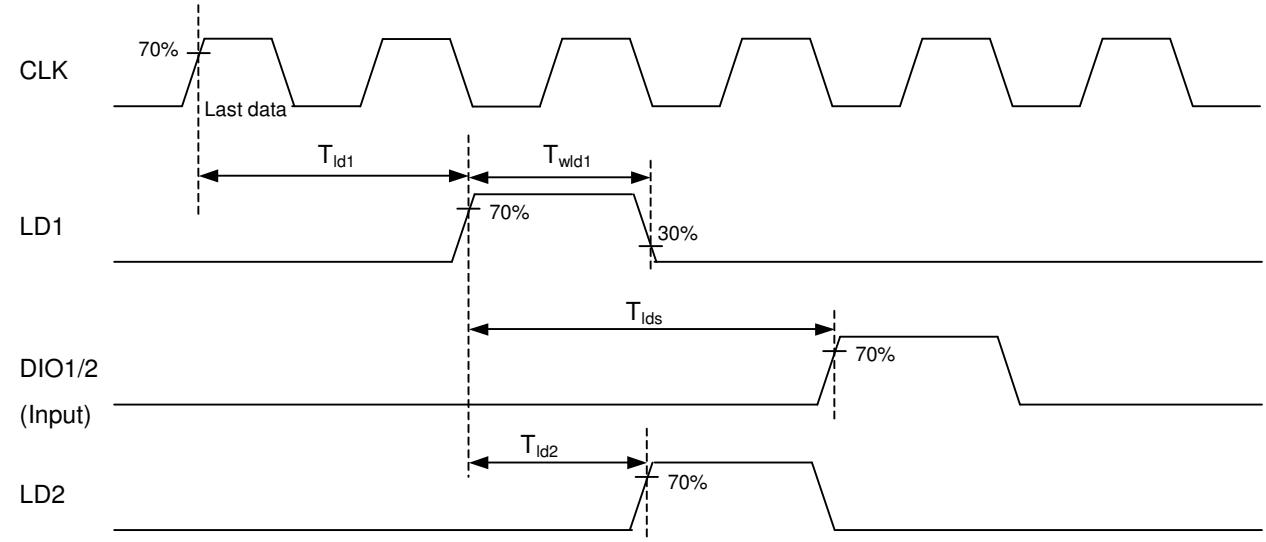


<< EDGSL= ”1”>>



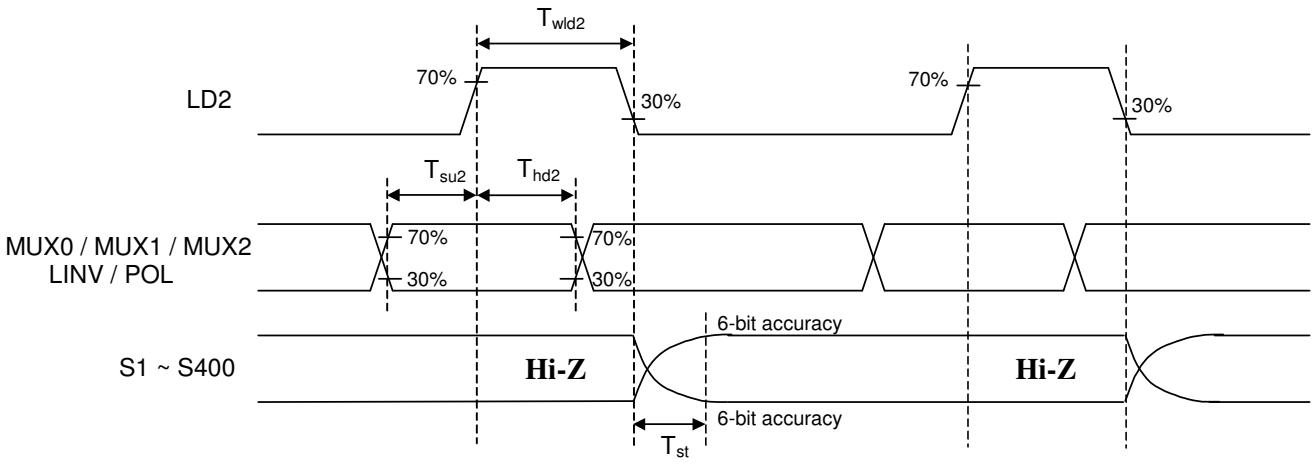
Timing Diagram 2

LD1 Timing Chart



Remark: During source output pre-charging are no relationship (Tld2) of the LD1 and LD2.

LD2 Timing Chart


T wld2
LD2
70%
30%
70%
30%
T su2
T hd2
MUX0 / MUX1 / MUX2
LINV / POL
70%
30%
70%
30%
6-bit accuracy
S1 ~ S400
Hi-Z
Hi-Z
6-bit accuracy
T st

E. Optical specifications

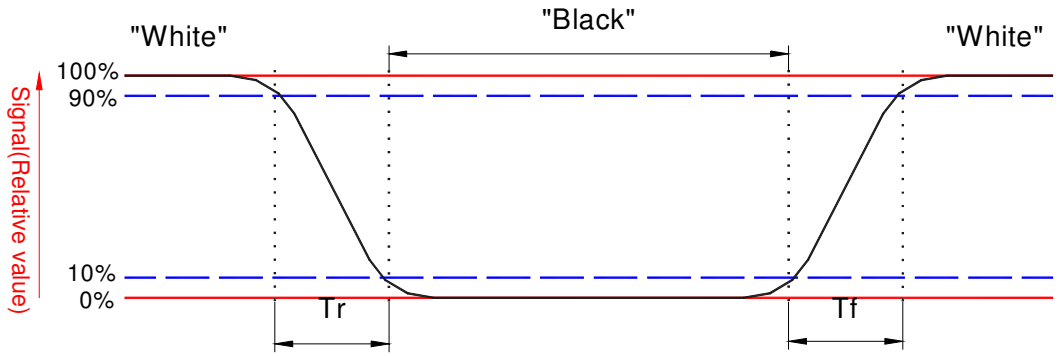
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise Fall	Tr Tf	θ=0°	- -	10 15	- -	ms ms	Note 3,5
Contrast ratio		CR	At optimized Viewing angle	200	300	-	-	Note 4, 5
Viewing angle	Top Bottom Left Right		CR≧10	- - - -	40 60 55 55	- - - -	deg.	Note 5
Brightness		Y_L	θ=0°	450	550	-	-	Note 1, 2, 6,7
White chromaticity		x	θ=0°	-	0.33	-	-	Note 1, 2, 6,7
		y	θ=0°	-	0.33	-	-	

Note 1: Ambient temperature =25±3˚C, Humidity=45～85％ RH, and LED current If = 150 mA. To be measured in the dark room under 10 Lux.

Note 2:To be measured on the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-7, after 15 minutes operation.

Note 3: Definition of response time:

The response time is defined as the time interval between the 10% and 90% of amplitudes. The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time).



Note 4. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

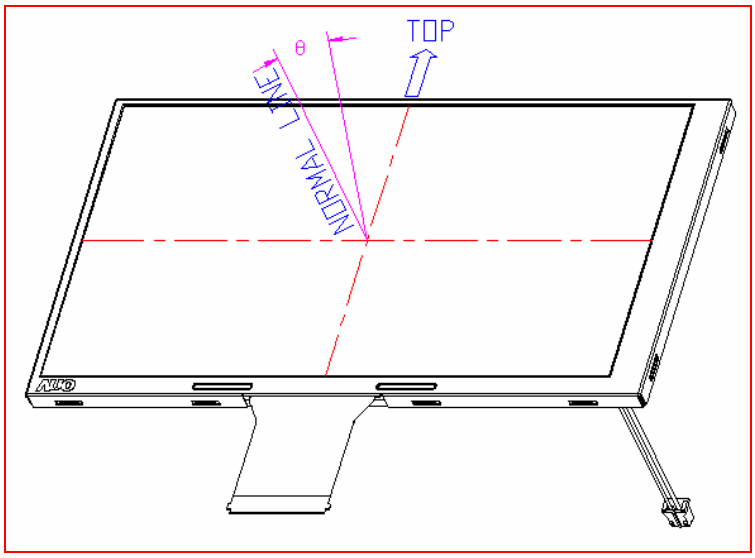
$$\frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Contrast ratio (CR)=

Note 5. Black reference voltage data =V1 or V4
White reference voltage data =V2 or V3
(For definition of V1, V2, V3 & V4, please refer to section I.1)
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 6. Brightness and White Chromaticity are measured at the display center.

Note 7. For definition of viewing angle please refer to figure as below.



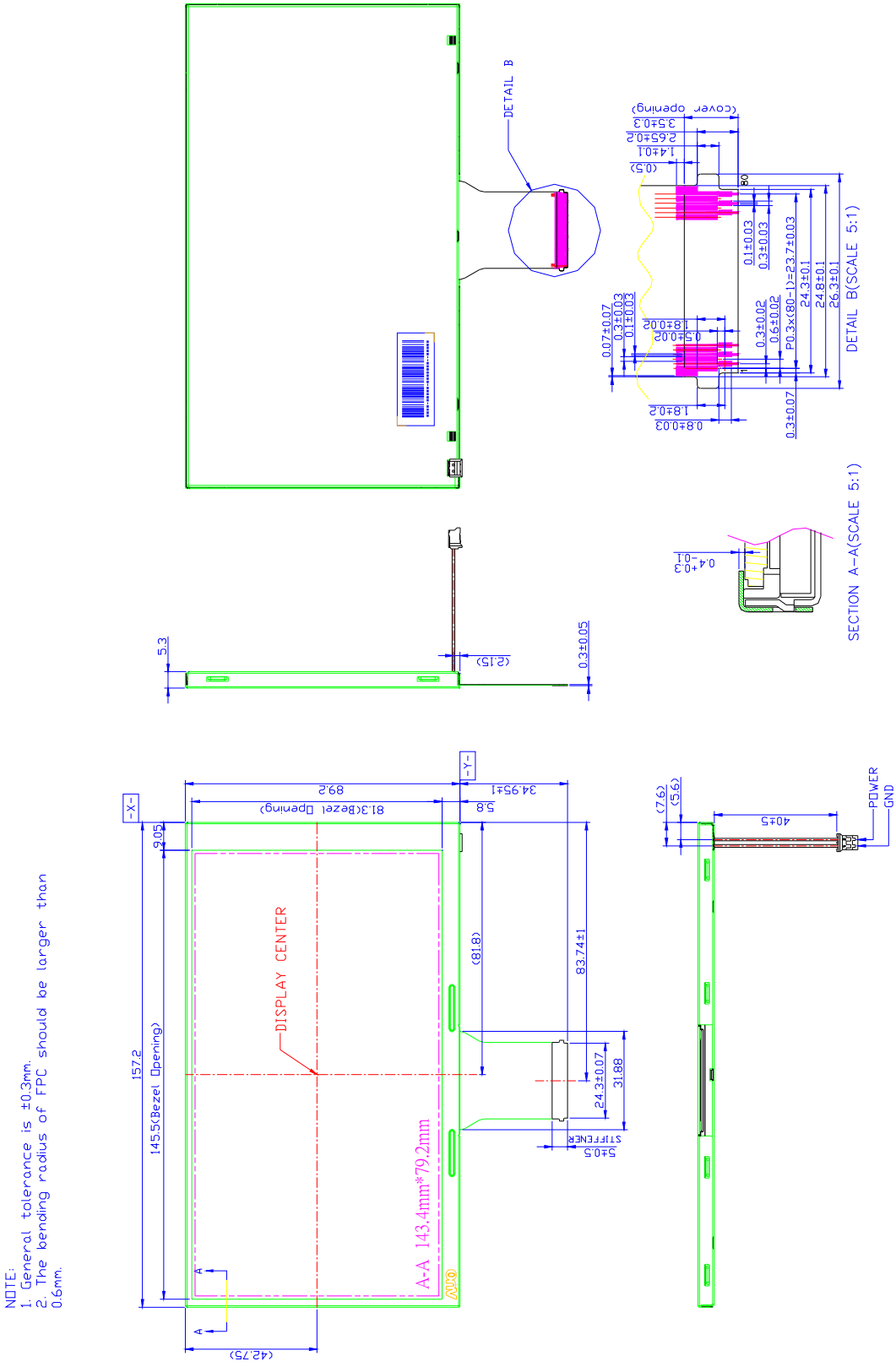
F. Reliability Test Items

No.	Test items	Conditions		Remark
1	High temperature storage	Ta= 95℃	240Hrs	
2	Low temperature storage	Ta= -40℃	240Hrs	
3	High temperature operation	Ta= 85℃	240Hrs	
4	Low temperature operation	Ta= -30℃	240Hrs	
5	High temperature and high humidity	Ta= 60˚C, 90% RH	240Hrs	Operation
6	Heat shock	-30˚C ~85˚C /100 cycles 1Hrs/cycle		Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω) once for each terminal		Non-operation
8	Vibration	Frequency range	8~33.3Hz	JIS D1601,A10 Condition A
		Stoke	1.3mm	
		Sweep	2.9G, 33.3~400Hz	
		Cycle	15min.	
		2 hours for each direction of X, Z 4 hours for Y direction		
9	Mechanical shock	100G, 6ms, ±X,±Y,±Z 3 times for each direction		
10	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz		IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces		

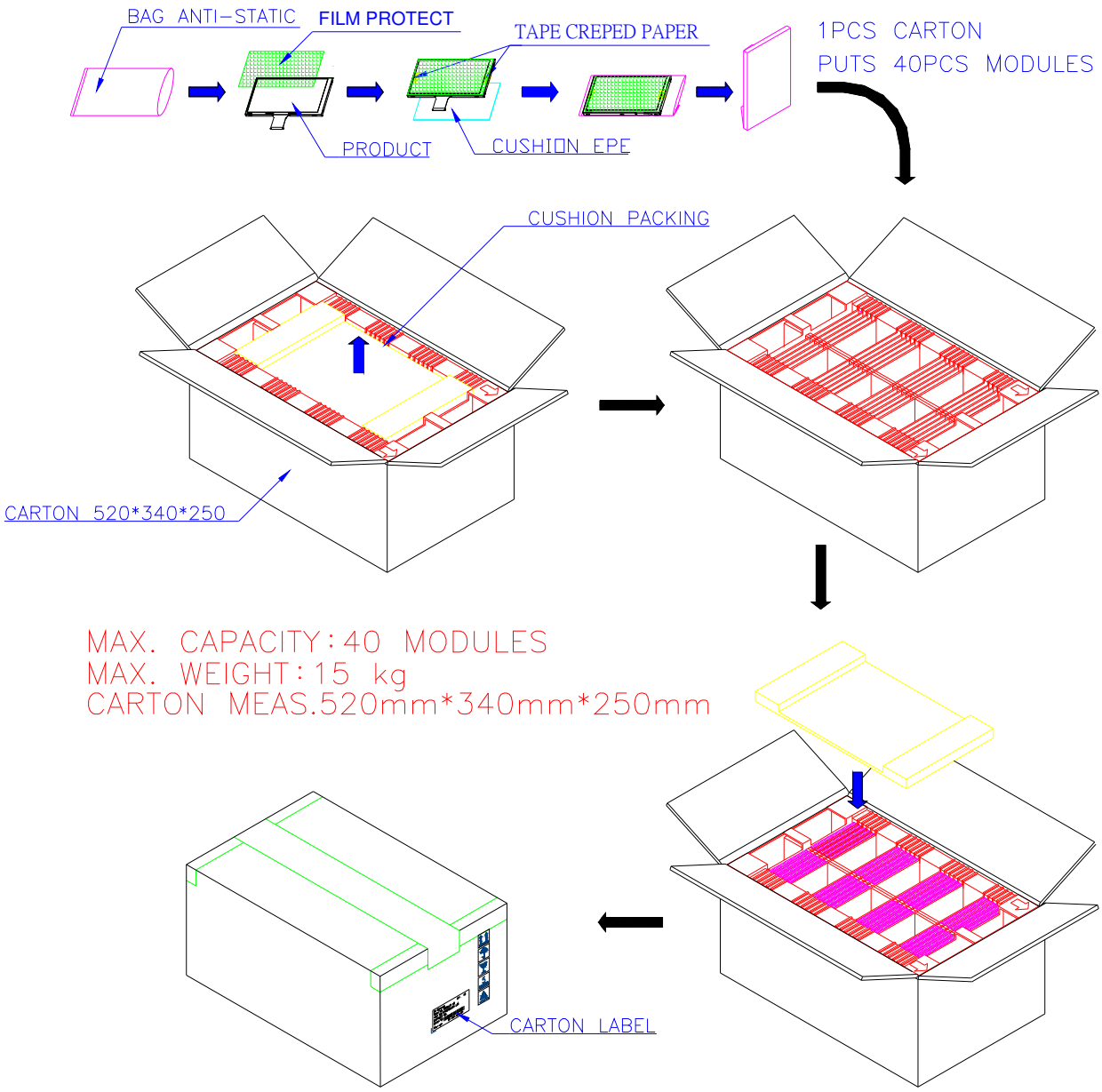
Note 1: Ta: Ambient temperature.

Note 2: In the standard conditions, no display function NG is allowed. All the cosmetic specification is judged before the reliability stress.

G. Outline Dimension



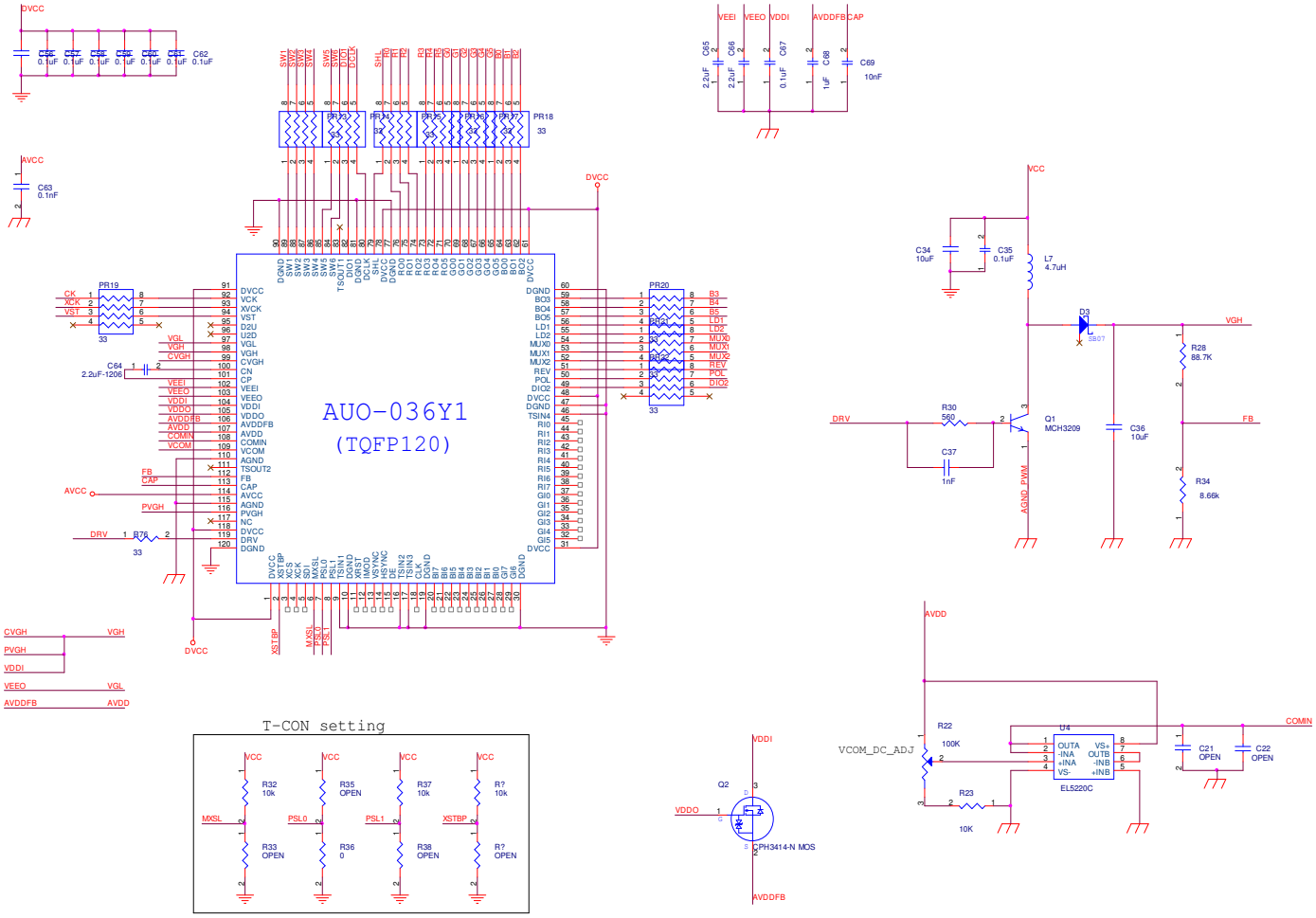
H. Packing Form



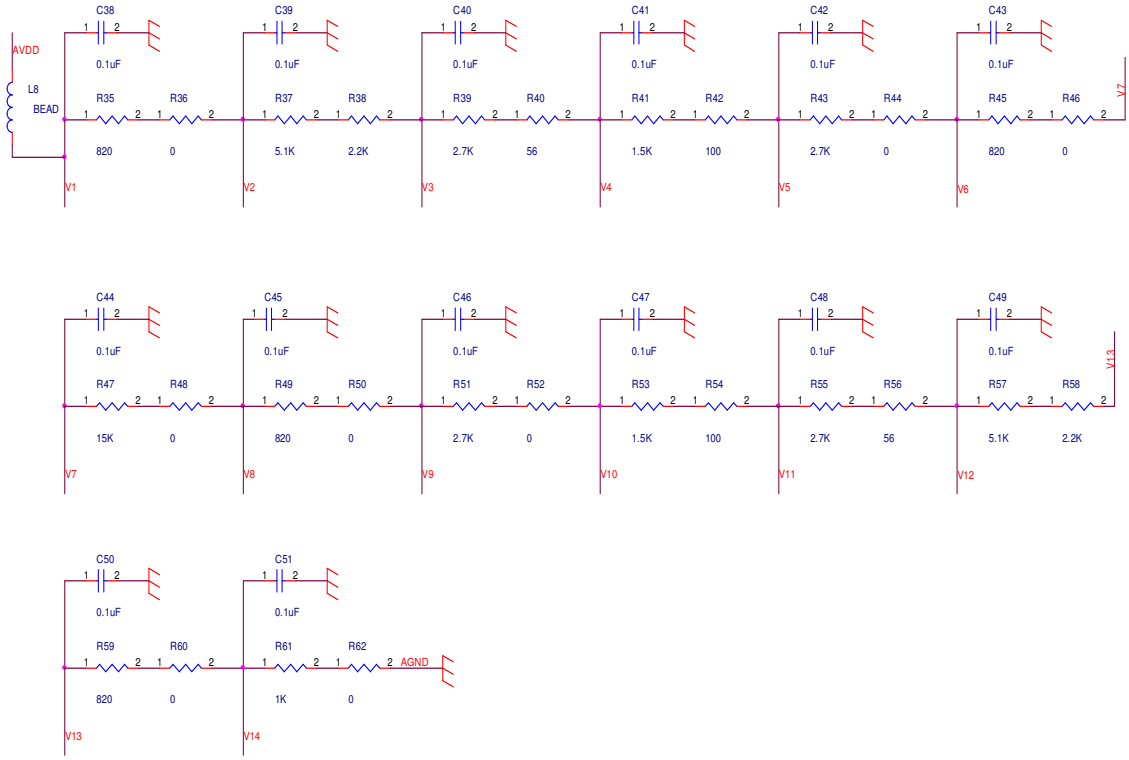
I.

J. Application Notes

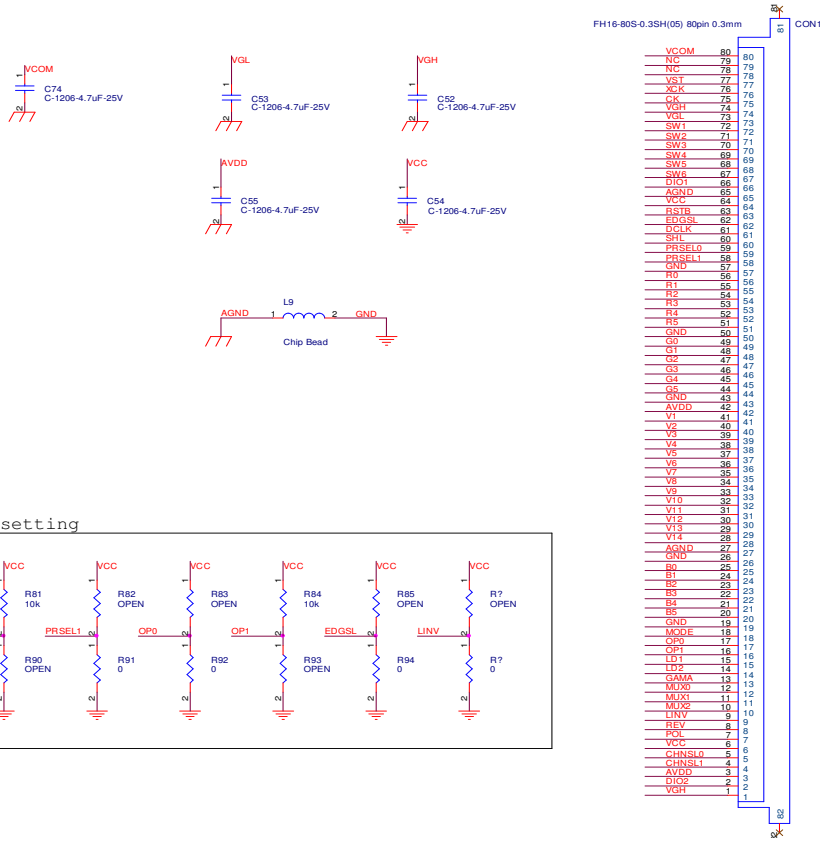
1. Typical Application Circuit



AUO-036 Circuit design

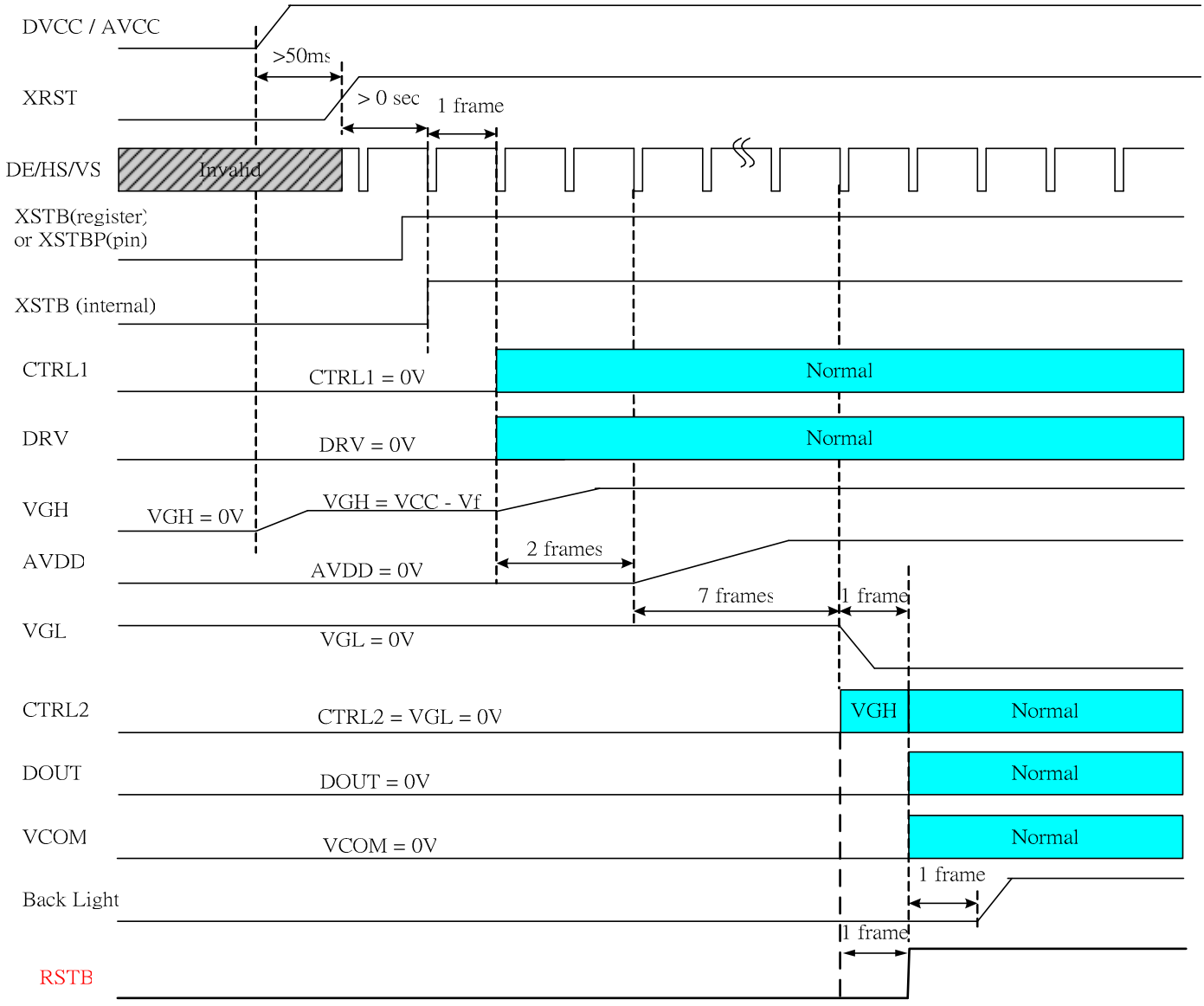


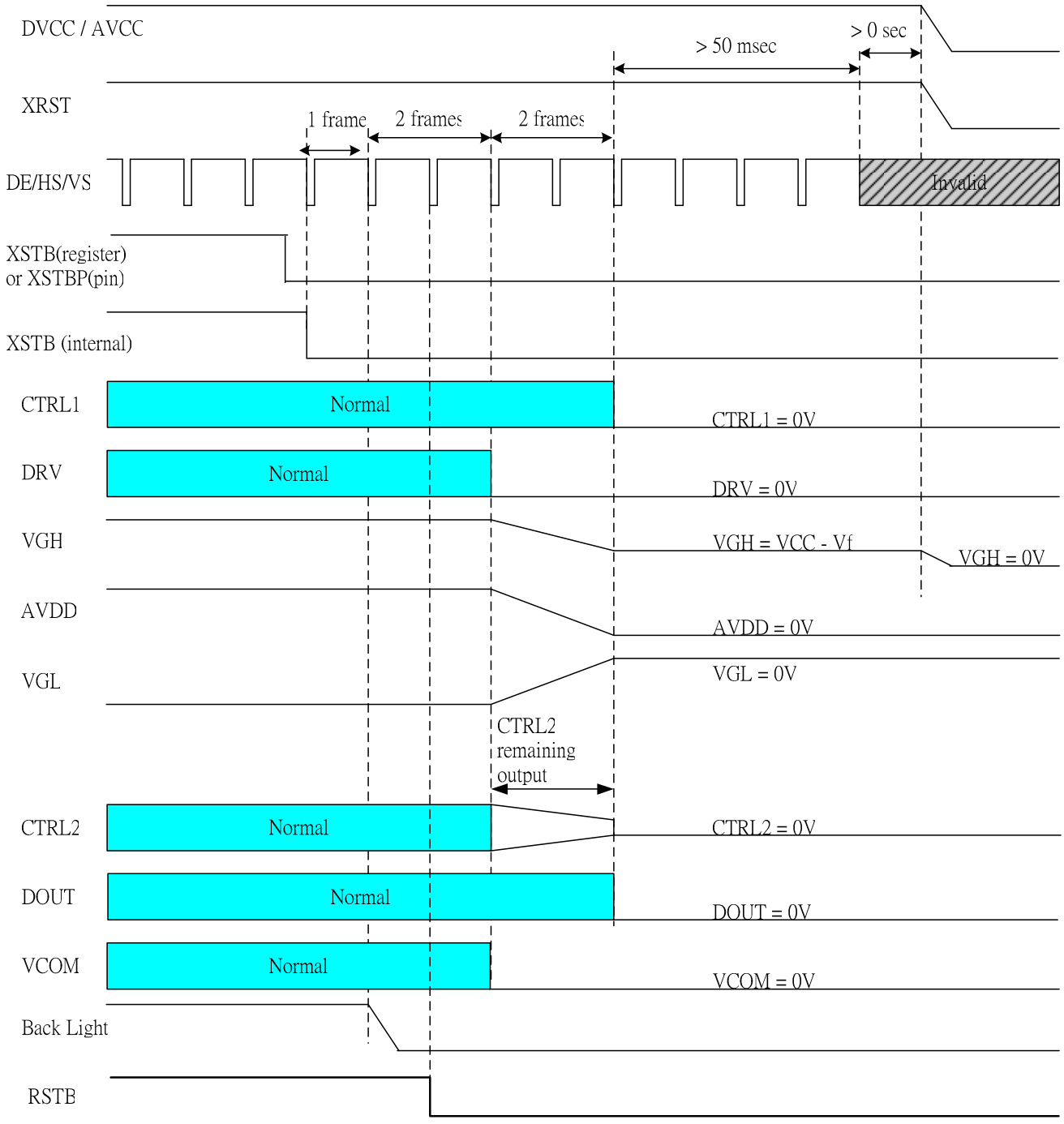
Gamma Circuit



Panel Setting

2. Power On/Off Sequence





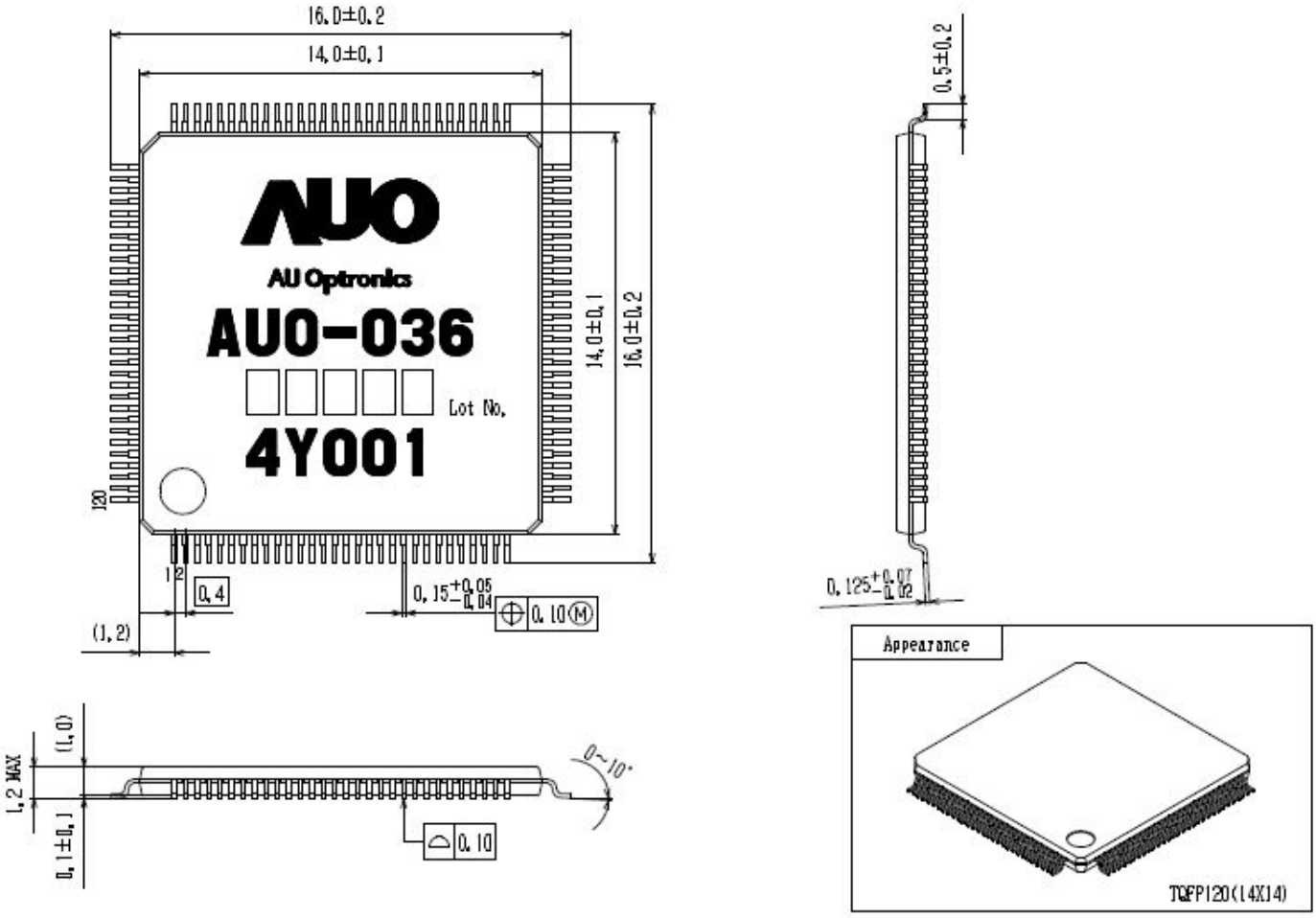
Note1: The using of standby mode signal XSTBP, please refer to AUO-036Y1 spec. P28.

Note2: Panel reset signal RSTB and ASIC reset signal XSTBP, please follow the power on/off sequence.

Note3: Input mode selection signal IMOD

IMOD="Low" : DE mode, please set VSYNC and HSYNC to "high".

IMOD="high" : HSYNC/VSYNC mode, please set DE to "low".



AUO-036 Package (TQFP120)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	DVCC	21	BI6	41	RI4	61	DVCC	81	DGND	101	CP
2	XSTBP	22	BI5	42	RI3	62	BO2	82	DIO1	102	VEEI
3	XCS	23	BI4	43	RI2	63	BO1	83	TSOUT1	103	VEEO
4	XCK	24	BI3	44	RI1	64	BO0	84	SW6	104	VDDI
5	SDI	25	BI2	45	RI0	65	GO5	85	SW5	105	VDDO
6	MXSL	26	BI1	46	TSIN4	66	GO4	86	SW4	106	AVDDFB
7	PSL0	27	BI0	47	DGND	67	GO3	87	SW3	107	AVDD
8	PSL1	28	GI7	48	DVCC	68	GO2	88	SW2	108	COMIN
9	TSIN1	29	GI6	49	DIO2	69	GO1	89	SW1	109	VCOM
10	DGND	30	DGND	50	POL	70	GO0	90	DGND	110	AGND
11	XRST	31	DVCC	51	REV	71	RO5	91	DVCC	111	TSOUT2
12	IMOD	32	GI5	52	MUX2	72	RO4	92	VCK	112	FB
13	VSYNC	33	GI4	53	MUX1	73	RO3	93	XVCK	113	CAP

14	HSYNC	34	GI3	54	MUX0	74	RO2	94	VST	114	AVCC
15	DE	35	GI2	55	LD2	75	RO1	95	D2U	115	AGND
16	TSIN2	36	GI1	56	LD1	76	RO0	96	U2D	116	PVGH
17	TSIN3	37	GI0	57	BO5	77	DGND	97	VGL	117	NC
18	CLK	38	RI7	58	BO4	78	DVCC	98	VGH	118	DVCC
19	DGND	39	RI6	59	BO3	79	SHL	99	CVGH	119	DRV
20	BI7	40	RI5	60	DGND	80	DCLK	100	CN	120	DGND

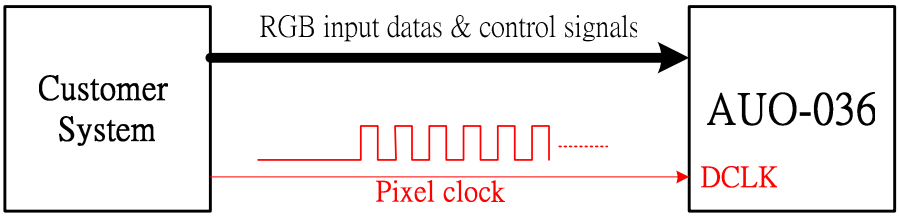
AUO-036 Pinout

Recommended register setting

		Register Data								Note
Reg NO.	Reg Name	D7	D6	D5	D4	D3	D2	D1	D0	
0	VDD_ADJ	X	X	X	0	1	1	1	1	VDD=11v
1	VEE_ADJ	X	X	X	X	0	1	0	0	(Default)
2	COMDC	1	0	0	0	0	0	0	0	(Default)
3	VPOSITION	0	0	1	0	0	0	0	0	(Default)
4	HPOSITION	1	0	1	0	0	0	0	0	
5	PANEL	X	1	1	0	0	0	0	1	
6	FUNCTION	X	X	X	1	1	1	0	1	
128	BLANK(1)	0	1	1	1	0	0	0	0	(Default)
129	PREC(1)	0	0	0	0	1	0	0	0	(Default)
130	SWITCH(1)	0	0	0	1	1	1	1	1	(Default)
131	INT(1)	0	0	0	1	1	0	0	0	(Default)
132	BLANK(2)	1	0	0	0	0	1	0	0	(Default)
133	PREC(2)	0	0	0	0	1	1	0	0	(Default)
134	SWITCH(2)	0	0	1	0	0	1	0	1	(Default)
135	INT(2)	0	0	0	1	1	1	0	0	(Default)
136	BLANK(3)	1	0	0	1	0	1	1	0	(Default)
137	PREC(3)	0	0	0	1	1	0	0	1	(Default)
138	SWITCH(3)	0	0	1	0	1	0	0	0	(Default)
139	INT(3)	0	0	0	1	1	1	1	0	(Default)

Important Note

1. In customer system, the initial state of the pixel clock output (DCLK pin of AUO-036) must be set to **Low**.



2. Please do not cut off the pixel clock during system operation.